## ABSTRACT

A circuit (1) comprising eight DACs (2a to 2h), the analog outputs of which are applied to the non-inverting inputs (6) of corresponding op-amps (7a to 7h) for gaining up the analog output voltage from the corresponding DAC (2). The op-amps (7) are identical, and are configured in a non-inverting mode with a closed loop gain of two provided by first and second resistors ($R_1$) and ($R_2$). Primary outputs (8) of the op-amps (7) are coupled to output pins (9a to 9h) of the circuit (1). The second resistors ($R_2$) couple primary inverting inputs (12) of the op-amps (7) to a common voltage reference rail (14), which is coupled to a true ground reference pin (15) through a coupling wire (16) which exhibit a combined inherent resistance ($R_p$). The voltage reference on the common voltage reference rail (14) varies with time as the output signals of the op-amps (7) vary, and would thus result in cross-talk between the DACs (2a to 2h). Each op-amp (7) comprises a secondary differential input amplifier stage (36), the non-inverting and inverting inputs (37,38) of which are coupled to the common voltage reference rail (14) and the ground reference pin (15), respectively. The secondary differential input stage (36) provides a secondary current to a node (29) in the op-amp (7) in response to variation in the time varying voltage reference for summing with an intermediate current provided through the node (29) by a primary differential input amplifier stage (25) of the op-amp (7) for correcting the output voltage signal on the primary output (8) for variation in the voltage reference on the common voltage reference rail (14).